Master 2 Internship

Towards New Frontiers in Multi-Core Response Time Analysis?

VERIMAG Laboratory (Grenoble, France) 2024–2025
Team **"Shared Resources"**
Advisors: Claire Maiza & Bruno Ferres
claire.maiza@univ-grenoble-alpes.fr
bruno.ferres@univ-grenoble-alpes.fr
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Context

Providing strong guarantees on the temporal bevahior of critical-systems is crucial in severous domains, such as avionics, aeronautics, automotive or nuclear. In order to do so, techniques have been developed to provide Worst-Case Execution Times (or WCET) of programs used in those critical systems, making it possible to bound the response time of the software on some processors – namely, on mono-core processors.
However, with the raising of multi- and many-core systems, it becomes more difficult to bound the response time of a given program, as it may interfere with other tasks at runtime. Analysis of the Worst Case Response Time (or WCRT) must hence consider not only the WCET of the task, but also the timing penalties that may occur due to the interferences of the other tasks (*e.g.,* cache and bus accesses, that may introduce unplanned delays). Last but not least, the analysis must also consider the hardware systems on which the software is being executed, as several aspects of the hardware can impact both the WCET and the interferences.
In this context, the Multicore Interference Analysis framework (or MIA) has been proposed in Verimag [1, 2]. This framework can be used to compute the WCRT of a given program, for a given hardware platform. It is based on a dual approach: WCET are computed with hypotheses on the interferences, then interference delays are computed and added to the response time. However, such approach relies on several abstractions, which might lead to over-pessimistic estimations of the global WCRT of the task.
In the context of the ANR project CAOTIC[1], we want to investigate how the dual-approach WCRT analysis could be improved. In particular, we think that the frontier between the WCET and the interference estimations could be refined, making it possible to tighten the bounds on the WCRT.

Goals of the Internship

The goal of this internship is hence to study how the WCRT analysis could be improved. In particular, we are interested in knowing if the over-approximations could be tackled in the WCET computation, in the interferences computation, or during the combination of both aspects.
The following contributions are hence expected:

- identify several execution scenarios where WCET and interferences are overlapping;

[1] **C**ollaborative **A**ctions **o**n **T**iming **I**nterferen**c**es, a research project funded by the **A**gence **N**ationale de la **R**echerche, led by Verimag.

- for each scenario:
    1. characterize the conditions leading to such overlapping;
    2. identify which analysis is responsible for the additional penalty in the WCRT;
    3. modify the analysis framework to tighten the WCRT.

Contributions are hence expected both on the theoretical aspects of the framework, and on the practical side, ideally leading to the improvement of the computed WCRT.

Ideal Applicant

This internship proposal is for Computer Science students at M2 level/last year of engineering school. The applicant must be proficient in the following knowledge/skills:

- micro-architecture of processors (*e.g.,* pipeline, cache policies, bus arbitration, ...)
- ability to read and understand research papers as well as technical documentation
- interest for verification methods (architecture modeling, WCET computation, ...)

As the MIA framework is written in `python`, good programming skills in this language would be appreciated.

Applications

To apply, send an email to claire.maiza@univ-grenoble-alpes.fr and bruno.ferres@univ-grenoble-alpes.fr, with your resume, a short covering letter, as well as any document that may support your application.

Location

The internship will take place in VERIMAG laboratory, located in the campus of Grenoble:

Laboratoire VERIMAG,
Bâtiment IMAG,
150 place du Torrent,
38401 Saint-Martin-d'Hères

Biblio.

[1] M. Schuh, *Safe Implementation of Hard Real-Time Applications on Many-Core Platforms*. PhD thesis, Université Grenoble Alpes, 2022. Available at https://theses.hal.science/tel-03827333.

[2] H. Rihani, *Many-Core Timing Analysis of Real-Time Systems*. PhD thesis, Université Grenoble Alpes, 2017. Available at https://theses.hal.science/tel-01875711.