# Postdoctoral Research position at Verimag: Modeling Power-Consumption of Systems-on-a-Chip in SystemC/TLM

## Scientific Context

### Transaction-Level Modeling of Systems-on-a-Chip:

The Register Transfer Level (RTL) used to be the entry point of the design flow of hardware systems, including systems-on-a-chip (SoCs). However, the simulation environments for such models do not scale up well. Developing and debugging embedded software for these low level models before getting the physical chip from the factory is no longer possible at a reasonable cost. New abstraction levels, such as the Transaction-Level Modeling, have emerged. The TLM approach uses a component-based approach, in which hardware blocks are modules communicating with so-called transactions. The TLM models are used for early development of the embedded software, because the high level of abstraction allows a fast simulation. This new abstraction level requires that SoCs be described in some non-deterministic asynchronous way, with new synchronization mechanisms, quite different from the implicit synchronization of synchronous circuit descriptions.

SystemC is a C++ library used for the description of SoCs at different levels of abstraction, from cycle accurate to purely functional models. It comes with a simulation environment, and became a standard (IEEE 1666). SystemC offers a set of primitives for the description of parallel activities representing the physical parallelism of the hardware blocks. The TLM level of abstraction can be described with SystemC.

### Power consumption:

The need for low-power systems is now well admitted, in the domain of embedded systems in general. This is particularly true for sensor networks or consumer electronics (mobile phones and all kinds of portable devices), because of lifetime constraints. But this is also true for other (non autonomous) embedded systems, in a world concerned with sustainable development.

Evaluating power-consumption early in the design flow, and therefore at a high level of abstraction such as TLM, is one of the challenges in the design of modern embedded systems.

## Verimag, STMicroelectronics and Docea Power Common Projects

Verimag and STMicroelectronics have been working together on TLM-related problems since 2002. The main problems we are looking at are the following:

- How to connect SystemC to formal verification tools? This was first adressed by the Ph.D of Matthieu Moy and is still an active research topic in the OpenTLM project.

- How to cover correctly the potential parallelism that is present in a SystemC design, and that is supposed to represent faithfully the physical parallelism of the hardware? The Ph.D of Claude Helmstetter adressed this problem with partial order reduction techniques.

- How to define precisely the nature of the information that should be present in pure functional models (also called TLM-PV, for "programmer's view") and in timed models (also called TLM-PVT, for "programmer's view + time")? How to construct a PVT model from a PV one without modifying its functionality, as seen by the developer of the embedded software? This was adressed by the Ph.D of Jerôme Cornet.

- How to define precisely what a TLM component should be, be it written in SystemC or not?

Docea Power is a start-up company specialized in power consumption and temperature analysis. Verimag started collaborating with Docea in march 2008 (See this webpage), and the collaboration continues in the HELP project.

## Objectives of the Post-Doc

The post-doc will work in the context of the HELP project. The main questions to address are:

- The best ways to connect a functional simulator with a tool for the analysis of non-functional properties (temperature, power-consumption). The current approach is to run the functional simulator, and let it dump a trace (typically in a text file). The non-functional analysis is done after-the-fact, based on this execution trace. This approach is limited since it does not allow a bi-directional communication between the functional simulator and the non-functional part (for example, a temperature sensor could hardly be modeled).

- How to write a "programmer's view + time + energy" based on a PVT model, without modifying its functionality. The existing approaches for power consumption analysis rely on annotation in the code of TLM program, but the PV level of abstraction does not always allow adding such annotations.

## Summary of expected work

We expect a novel approach to answer the two questions above. The approach will first be experimented on a small example in SystemC. It will then be validated on a real industrial case study, provided by STMicroelectronics.

## Required Skills

The ideal candidate should have a Ph.D degree in computer science, combine solid theoretical background and software development skills, and have some degree of autonomy. Good English speaking and writing skills are required (French is not required). The candidate should be able to work in a collaborative environment, with a strong commitment to reaching research excellence and achieving assigned objectives.

In depth previous experience in the following areas is required:

- C++ (some knowledge of SystemC and/or TLM would be appreciated)

- Modeling/virtual prototyping of systems

## Terms of employment

A full-time position as a postdoctoral researcher for a period of 24 months starting as soon as possible after May 1st, 2010.

The salary will be 2500 EUR gross per month depending on qualifications and experience.

# Application

Send a detailed CV, a list of publications, a list of referees (persons that can recommend you), and a short letter explaining your motivations for this position, by email to:

Florence.Maraninchi@imag.fr, Matthieu.Moy@imag.fr, Karine.Altisen@imag.fr

Please include [POSTDOC HELP] in the subject of your mail, and only attach **PDF** files.

Send your application as soon as possible, and no later than **October 31th, 2010.**